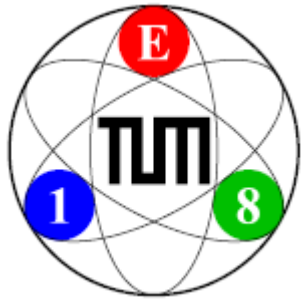


FPGA based Data Acquisition and readout systems of PENELOPE, Belle2 pixel Detector, and COMPASS

Igor Konorov
TUM Physics Department E18

Detector workshop
Garching, May 30-th – June 1-t 2016

Talk overview

- Modern FPGA architecture
- Requirements of distributed readout systems
- Unified IP cores(libraries)
  - IPBUS
  - Time distribution system => Unified Communication Framework
- PENELOPE
- Belle II DEPFET detector readout system
- FPGA event builder of COMPASS DAQ

FPGA

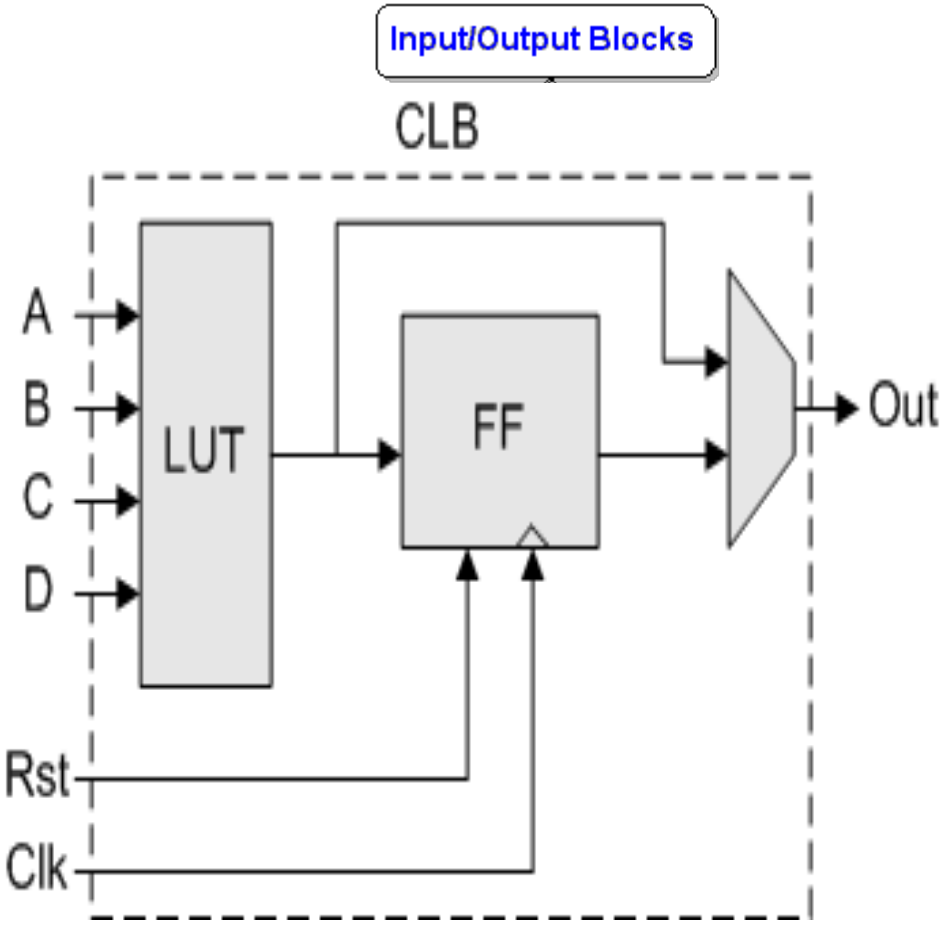
Field Programmable Gate Array

Field Programmable Gate Array

2D structure of Configurable Logic Blocks
Programmable interconnect
- Good connection between neighboring CLBs
- Extended long connections

Programmable IO cells

Configuration information stored in Static Memory
FPGA to be programmed every time after power up



Why to use FPGA

- Adaptive interfaces to ASICs, ADCs, TDCs…
- Typical processing clock 100-200 MHz
- Pipe line data processing
- Parallel architecture => multiple pipelines

Modern FPGA features

- Delay Locked Loop, Phase Locked Loop
- Memory blocks (RAM/FIFO)

- **Multiple High speed serial links up to 28 Gbps !!!!**
  - MAC cores for 1/10/40/100 Gigabit Ethernet
  - PCIexpress Gen1-Gen3

- Soft core SDRAM controllers support up to 800 MHz bus frequency => 6.4GB/s
- Hard core SDRAM controllers support up to 2000 MHz bus frequency => 16 GB/s

Logic Density FPGA vs CPU/GPU

Chip	Manufacturer	Technology	Transistor count
Duo-core + GPU Iris Core i7 Broadwell-U	Intel	14 nm	1 900 000 000
22-core Xeon Broadwell-E5	Intel	14 nm	7 200 000 000
Virtex 7	Xilinx	28 nm	6 800 000 000
Virtex Ultra Scale	Xilinx	20 nm	20 000 000 000

FPGA performance parameters

Low cost FPGA (Artix7)

- Memory 1.4MByte
- GBT 100 Gbps

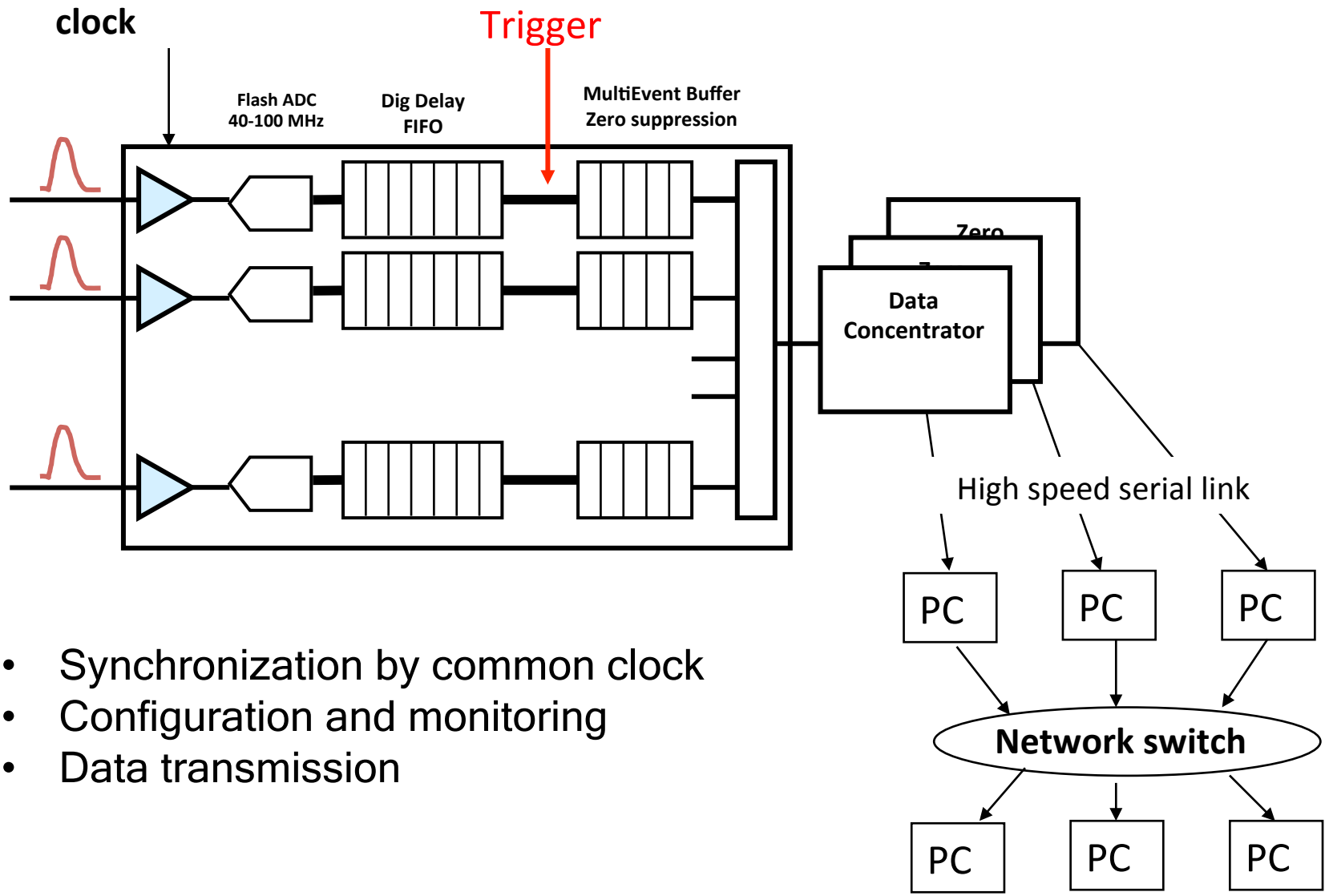
High end FPGA (UltraScale)

- Memory 14 Mbyte
- GBT 3000Gbps

Architecture and requirements of modern experiments

Igor Konorov, TUM

Pipelined DAQ



- Synchronization by common clock
- Configuration and monitoring
- Data transmission

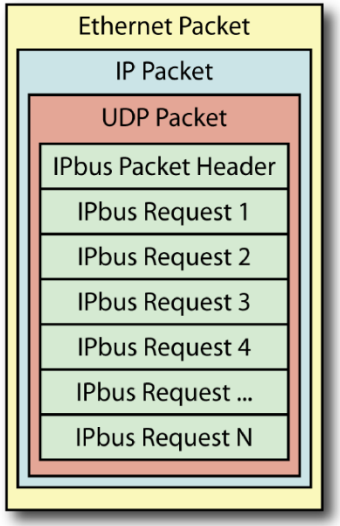
FE/DAQ Interfaces

- Time reference system
  - Common clock
  - Trigger, event number and other info distributed together with clock
  - TCS for COMPASS, B2TT for Belle II
  - TCS/B2TT => FPGA (custom interface)

- Slow control interface
  - Configuration front-end and DAQ electronics;
  - Monitoring : temperature, voltages, currents;
  - IPBUS => PC ⇔ FPGA interface

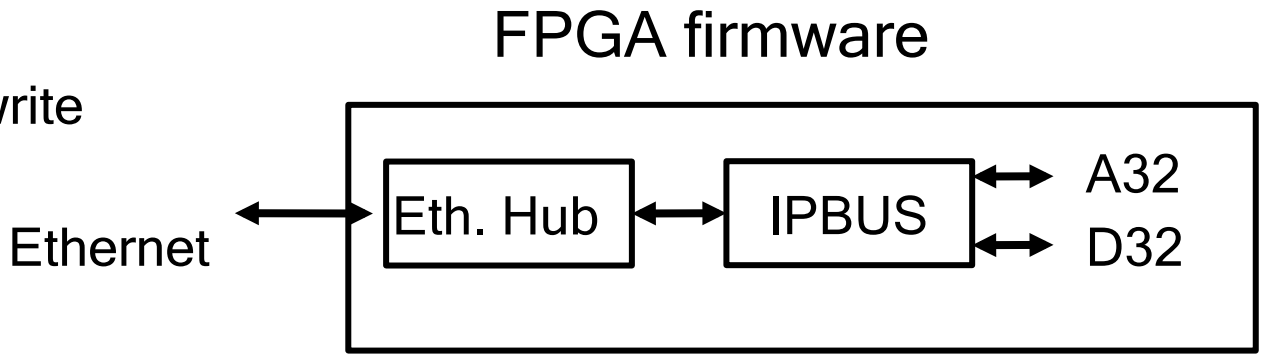
IPBUS

Developed by CMS to access FPGA in ATCA/uTCA
Ethernet (UDP based) protocol
https://svnweb.cern.ch/trac/cactus/wiki/uhalQuickTutorial
µHAL: c++ framework
Pycohal: python bindings
Supported by EPICS



IPBUS:

- Access virtual uP bus in FPGA
- 32 Address, 32 data
- 3 types of transactions
  - read
  - write
  - read-modify-write



FE/DAQ Interfaces

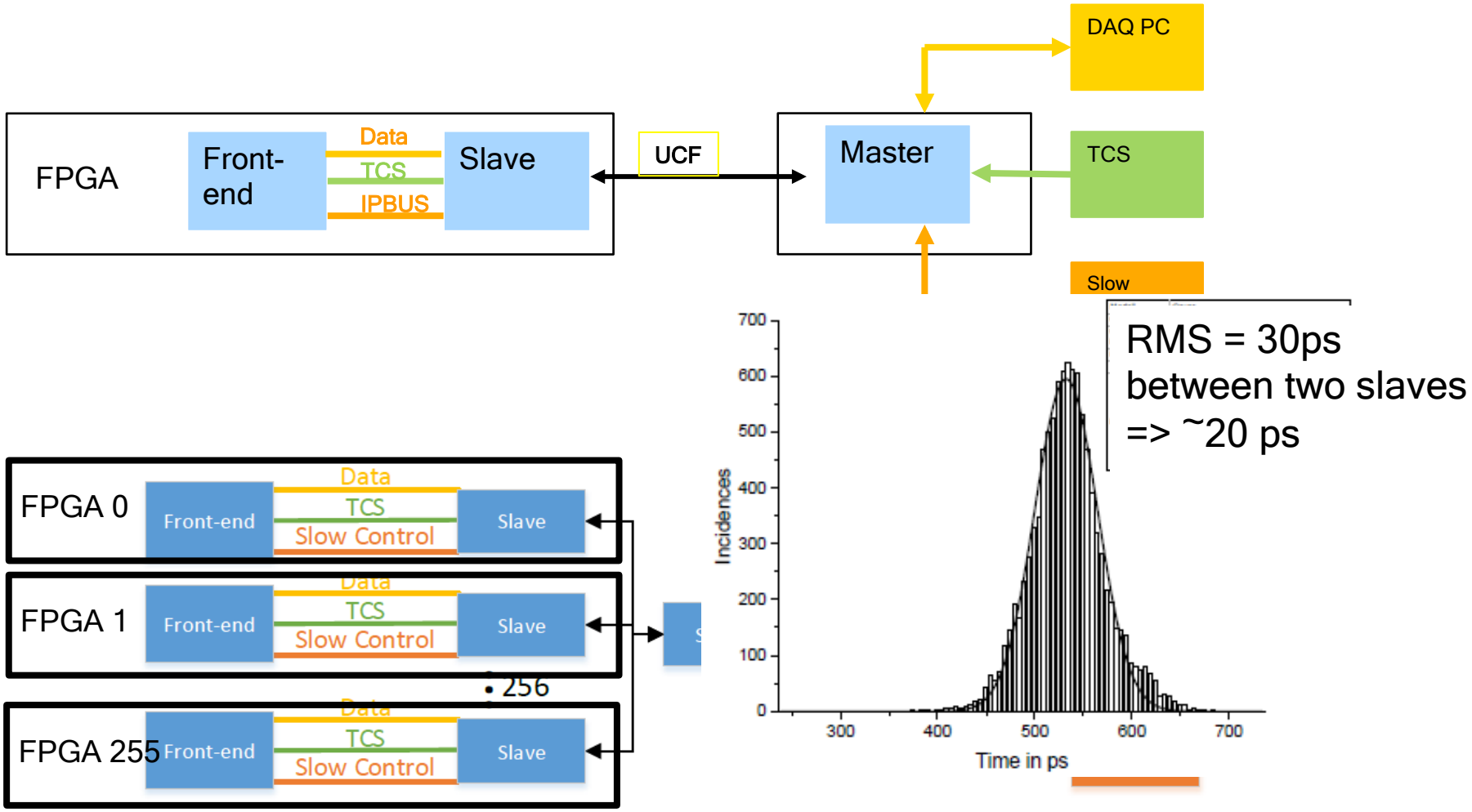
- Time reference system
  - Common clock
  - Trigger, event number and other info distributed together with clock
  - TCS for COMPASS, B2TT for Belle II
  - TCS/B2TT => FPGA (custom interface)

- Slow control interface
  - Configuration front-end and DAQ electronics;
  - Monitoring : temperature, voltages, currents;
  - IPBUS => PC ⇔ FPGA interface

- Data transmission interfaces
  - High speed serial links : Slink(CERN) , Aurora(Xilinx), UDP

- For our electronics we developed UCF(Unified Communication Framework)
  - Provides infrastructure for all three interfaces within single serial link(fiber) for FPGA ⇔ FPGA

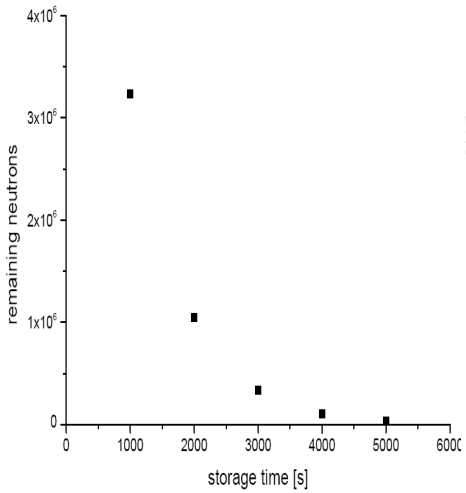
Unified Communication Framework

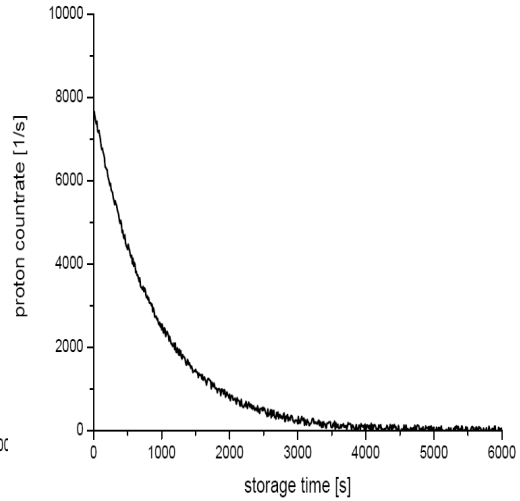


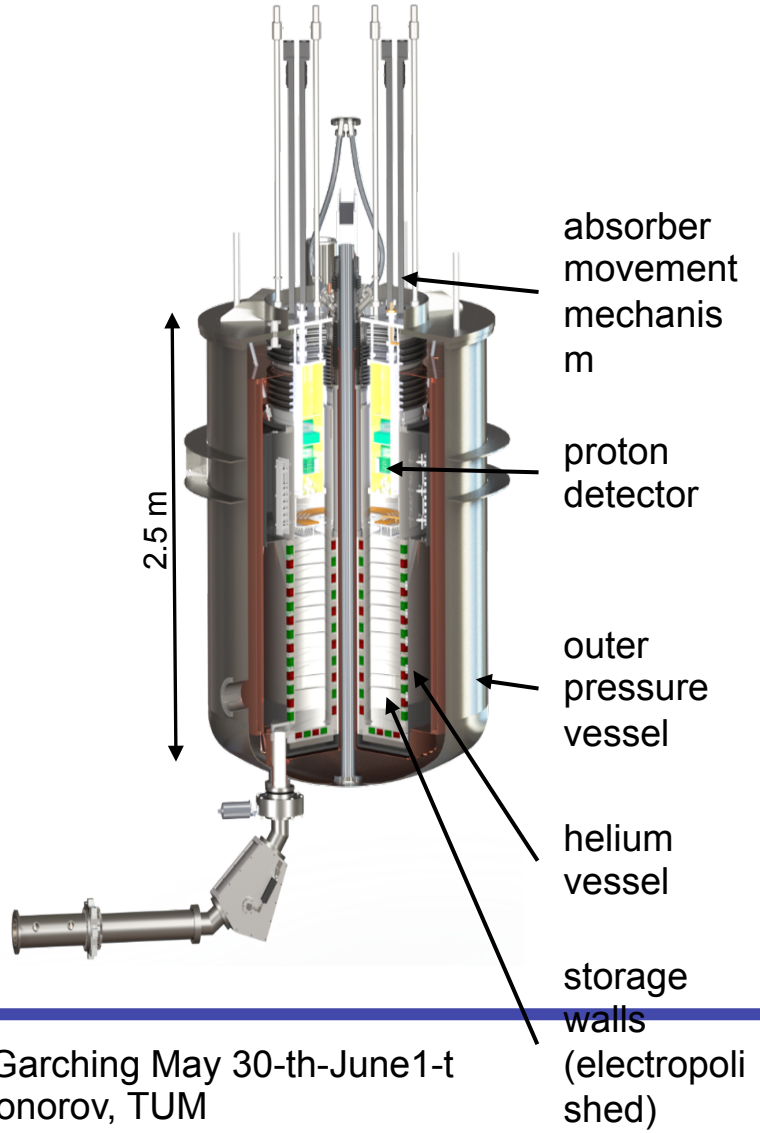
PENELOPE

PENeLOPE

- **P**recision **E**xperiment on **Ne**utron **L**ifetime **O**perating with **P**roton **E**xtraction
- Will be located at the Forschungs-Neutronenquelle Heinz Maier-Leibnitz (FRM II)
- Magneto-gravitational trap for ultra-cold neutrons
- Aiming for a precision of ± 0.1 s
- Measuring protons and neutrons

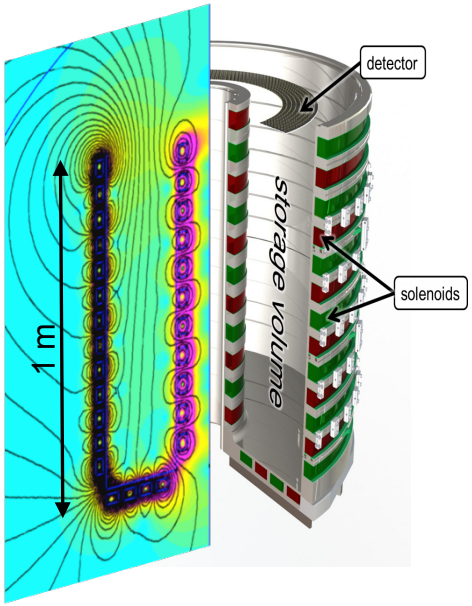


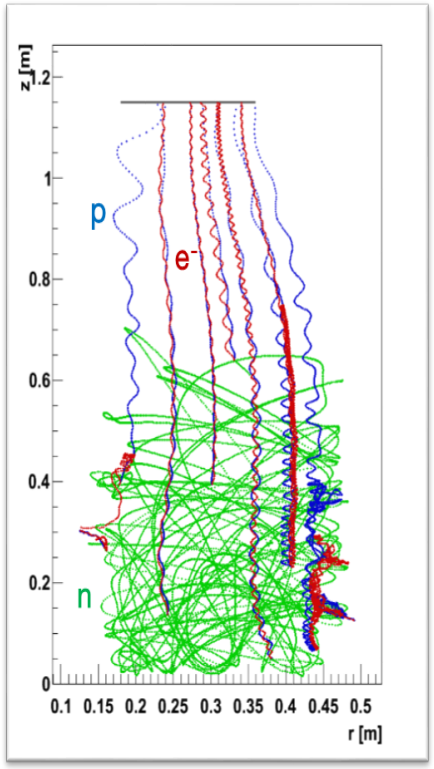




Proton Detector Requirements

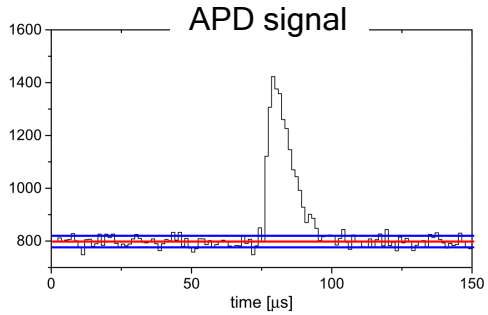
- Protons are guided via magnetic and accelerated by electrical field
- Complete Electronics on -30 kV
- APDs at 77 K
- Active area of 0.23 m^2
- ~2000 APDs to be readout
- Peak event rate per channel: ca. 70 p/s + 35 e^-/s + γ = 105 events/s + bg
- Average event rate: 130.000 events/s + bg ≈ data rate: 500 Mbit/s
- Background is < 1/Ch/s

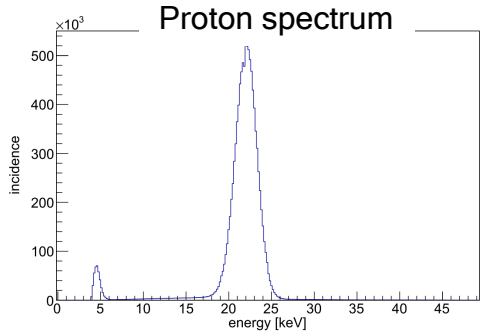


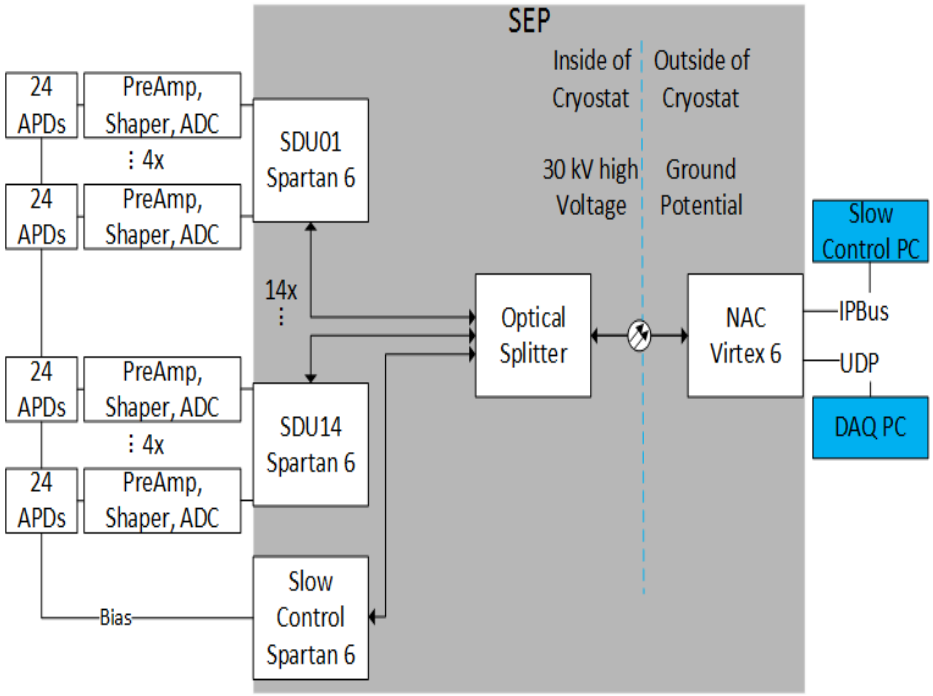


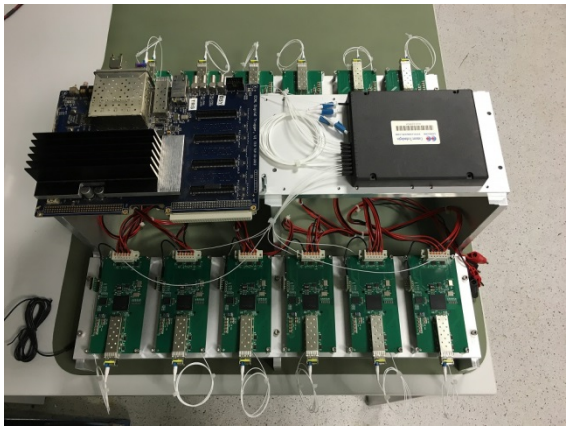
Proton Detector Readout Concept

- APD signal detected, processed, and readout
- Data driven readout
- UCF : Single fiber interface, time sharing, similar to common bus
- UDP readout





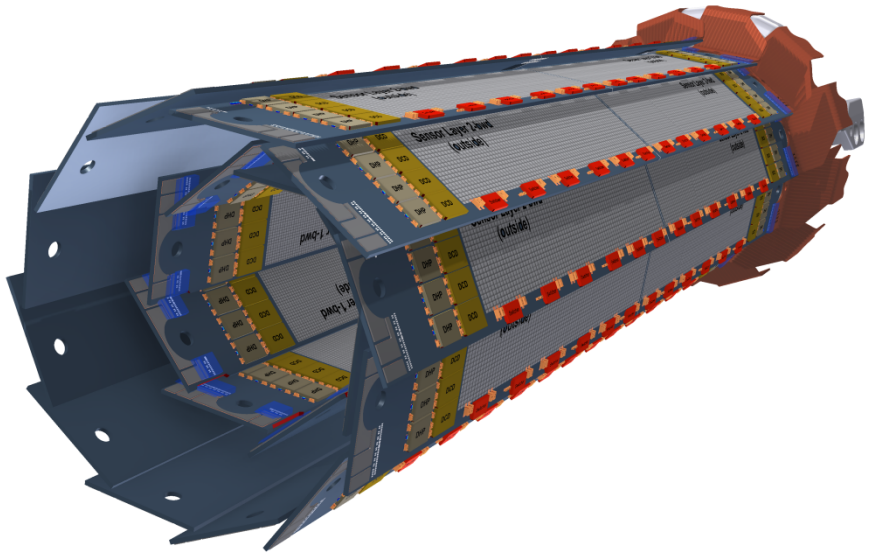




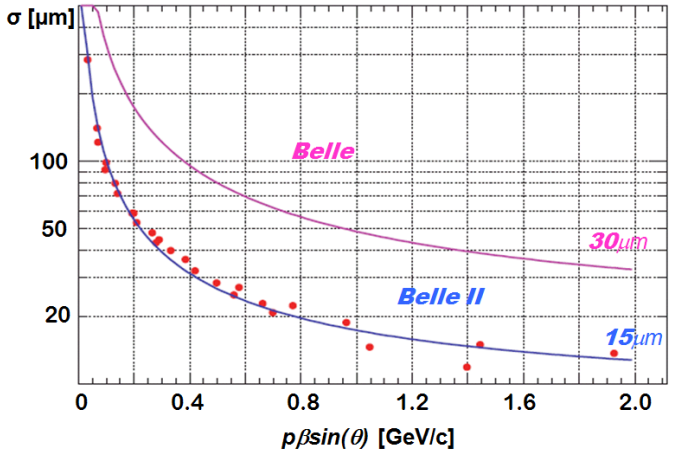
DEPFET pixel detector
For Belle II

Igor Konorov, TUM

DEPFET PXD detector



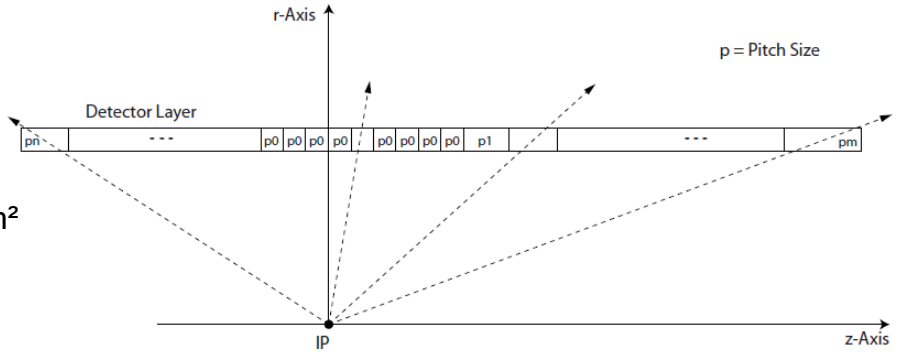
Impact parameter resolution



DEPFET PXD, sensors developed by HLL

- Two layers :
  - L1 : 8 inner layers, 1.4 cm from IP, 44.8 x 12.5 mm²
  - L2 : 12 outer layers, 2.2 cm from IP, 61.44 x 12.5 mm²

- 40 half ladders => Half ladder 250x768 pixels => 7.68 Mp
- 75 um thick



Total material budget 0.2% X/X_0

PXD Read Out

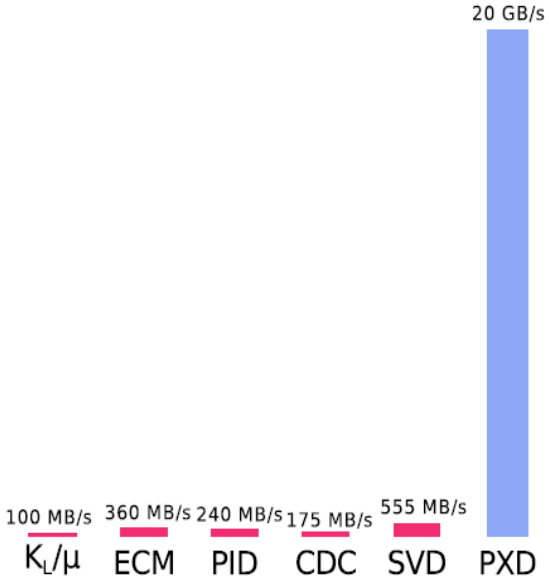


Figure : Data rates in Belle 2

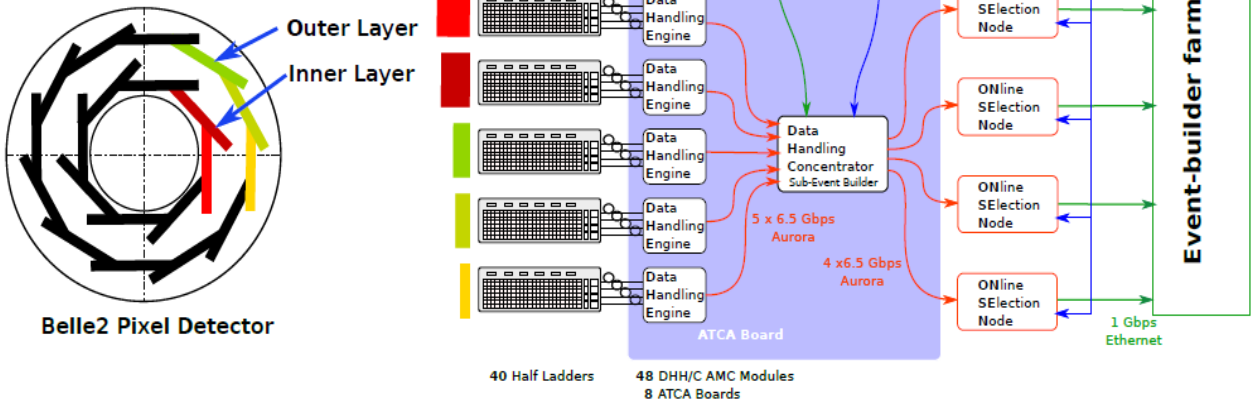
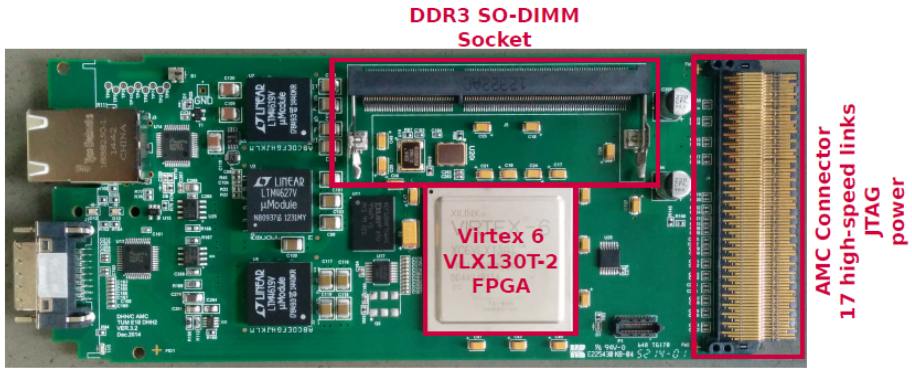


Figure : Data read-out chain

One Carrier card (ATCA) performance : 2.5 GB/s data throughput
PXD DAQ : 8 x DHH Carrier Cards
20GB/s before HLT and 1BG/s after

DHH system prototype



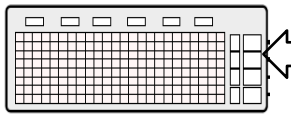
- V6 VLX130T
- 17 High speed links (17x6.5Gbps)
  - IPBUS
  - UDP
  - 4xAurora
  - ..
- 4GB of memory

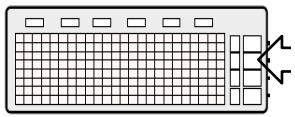
DHH at DESY test beam

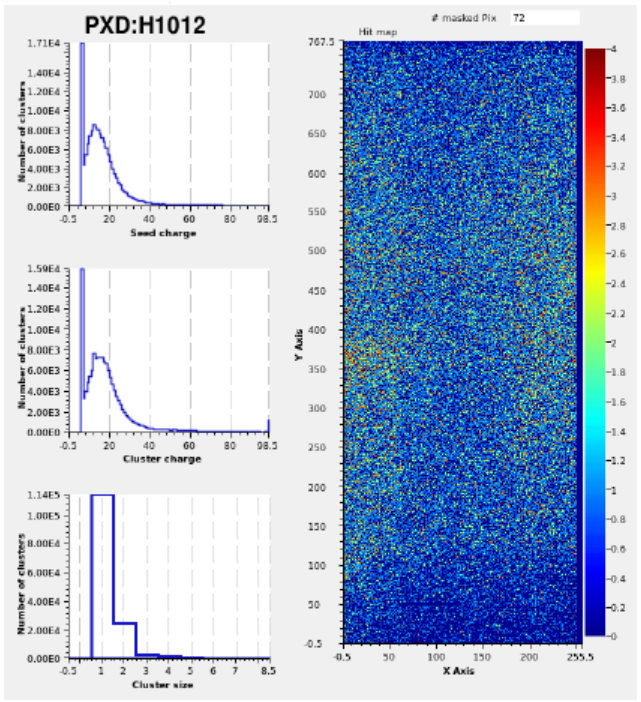
Trigger
127MHz

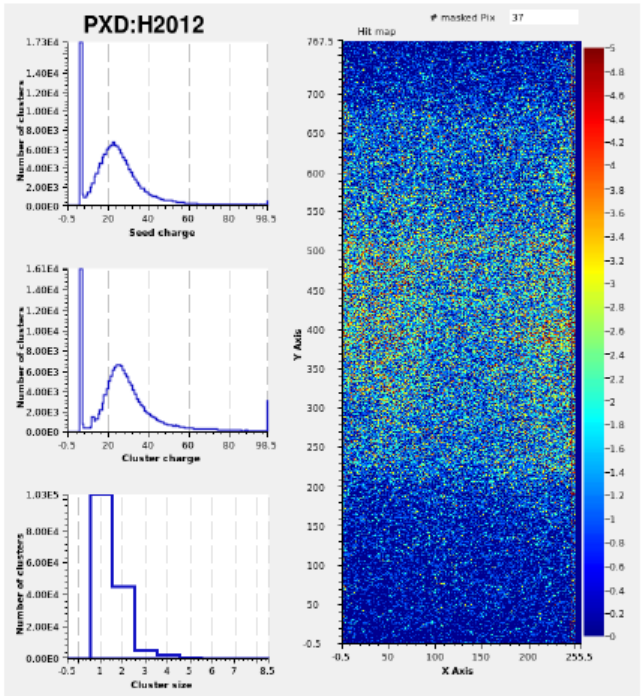
B2TT

EPICS









→ DAQ

Local DA(

- Pe
- DQM during data taking
- Generate log file of data consistency check

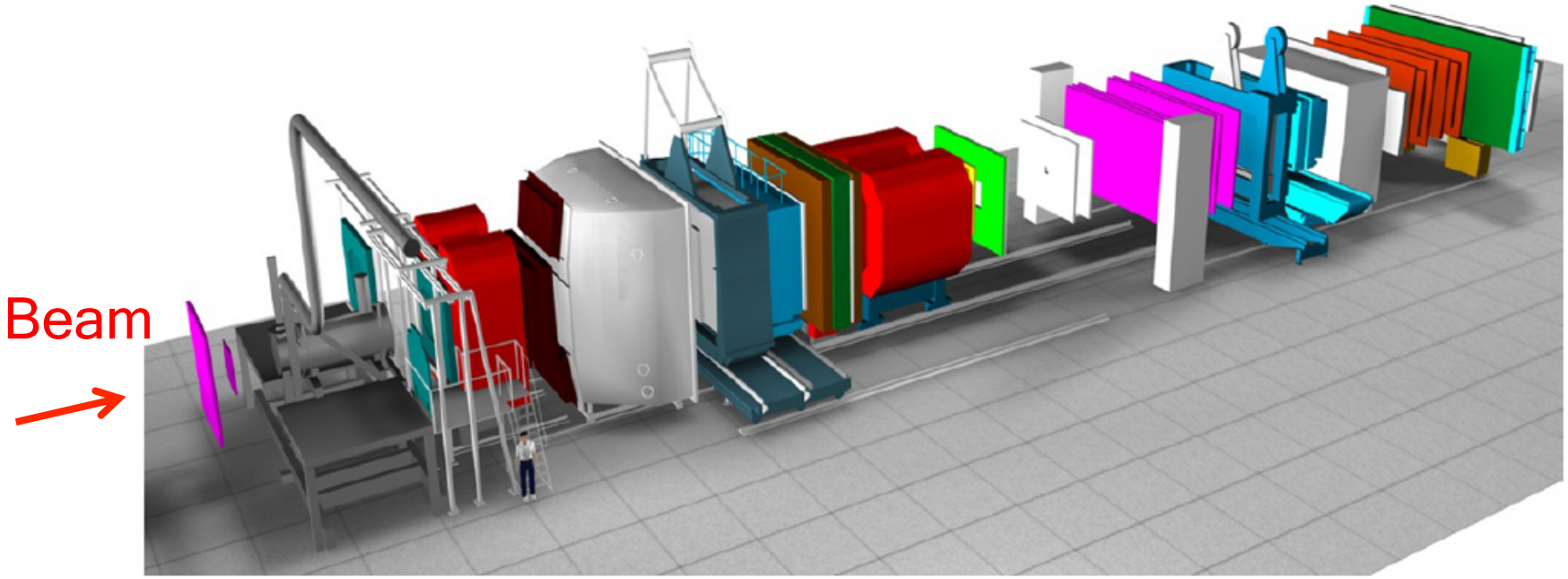
COMPASS EVENT BUILDER FPGA

Igor Konorov, TUM

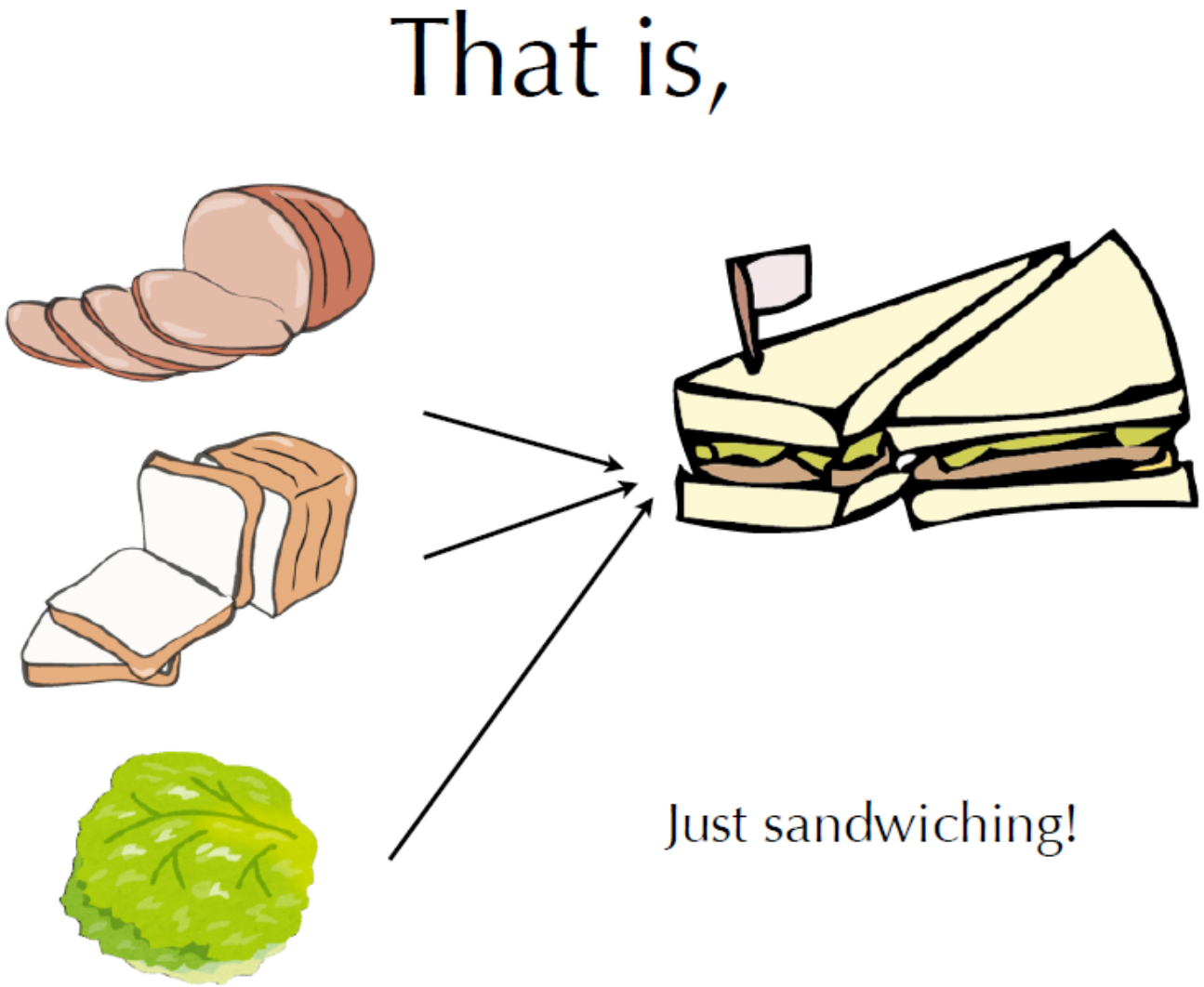
COMPASS Experiment overview

Length : 60m
Detector channels : 300 000
Trigger rate : 30kHz
In spill data rate : 1.5GB/s
Sustained rate : 400MB/s

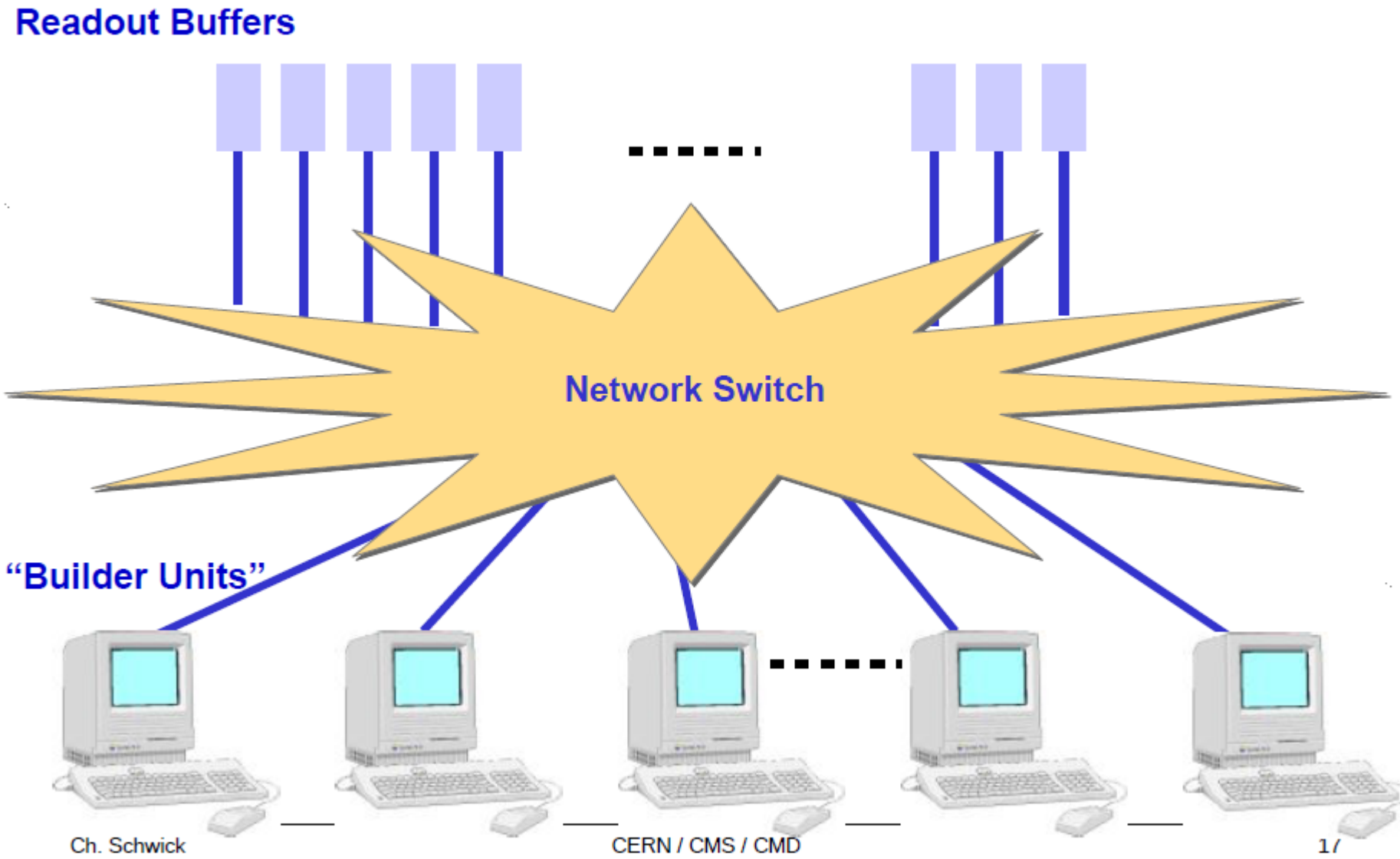
- Fixed target experiment at SPS CERN
- Beams: $4\ 10\uparrow 7\ \mu s\uparrow -1$, $2\ 10\uparrow 7\ hadrons\ s\uparrow -1$
- Since 2012 COMPAS II
- Physics case : Drell-Yan, DVCS
- FPGA event Builder since 2014



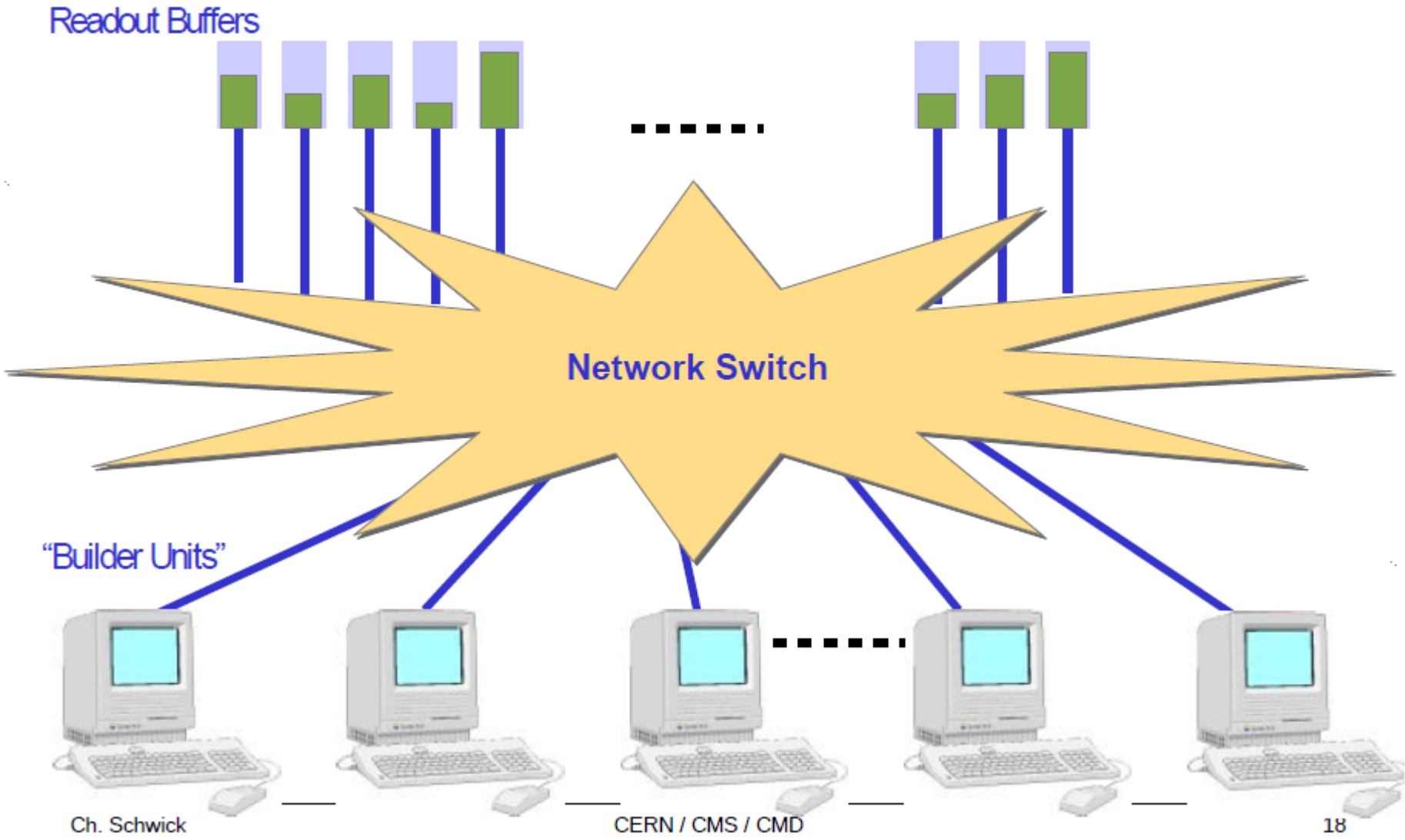
What is Event Building



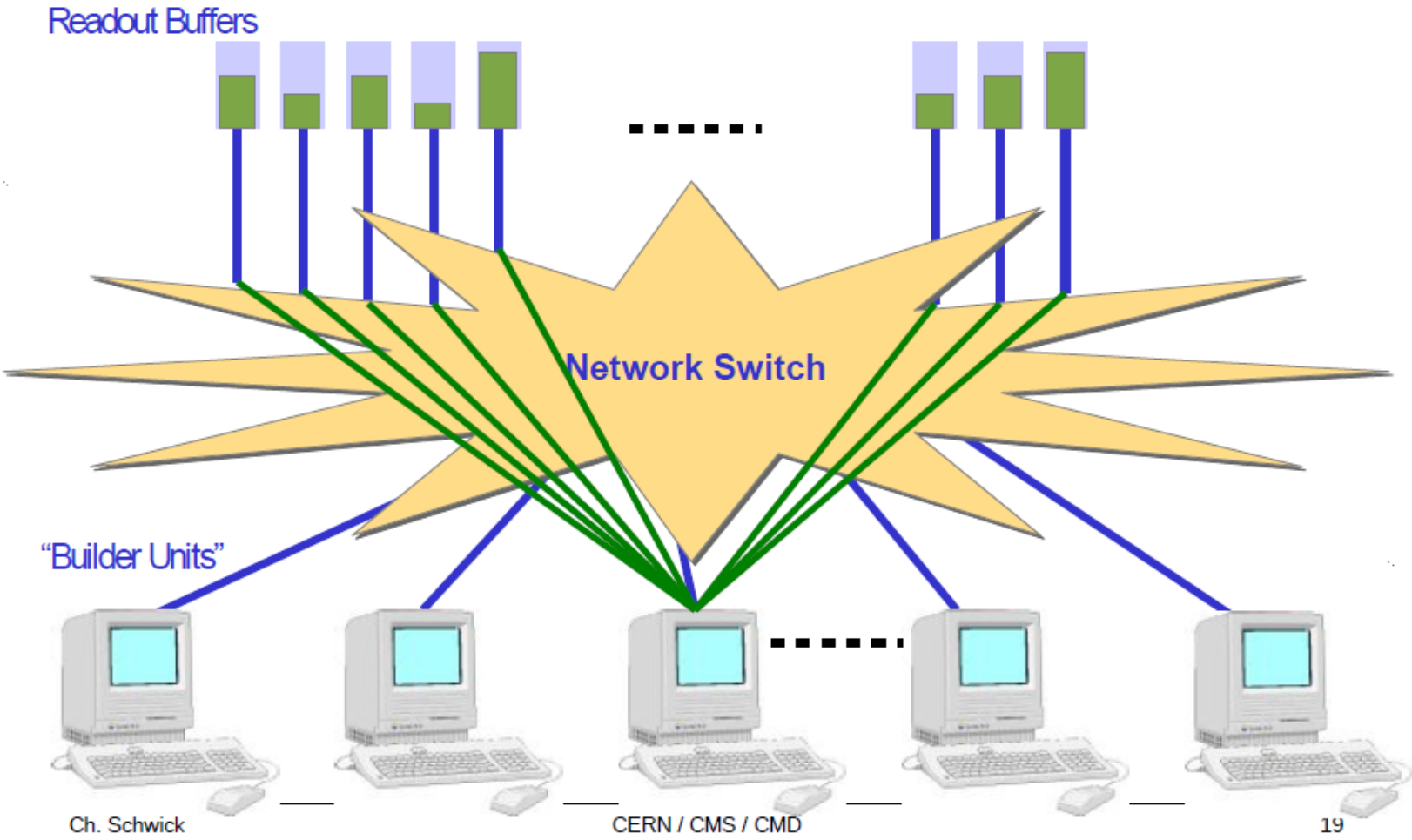
Networking: EVB traffic



Networking: EVB traffic



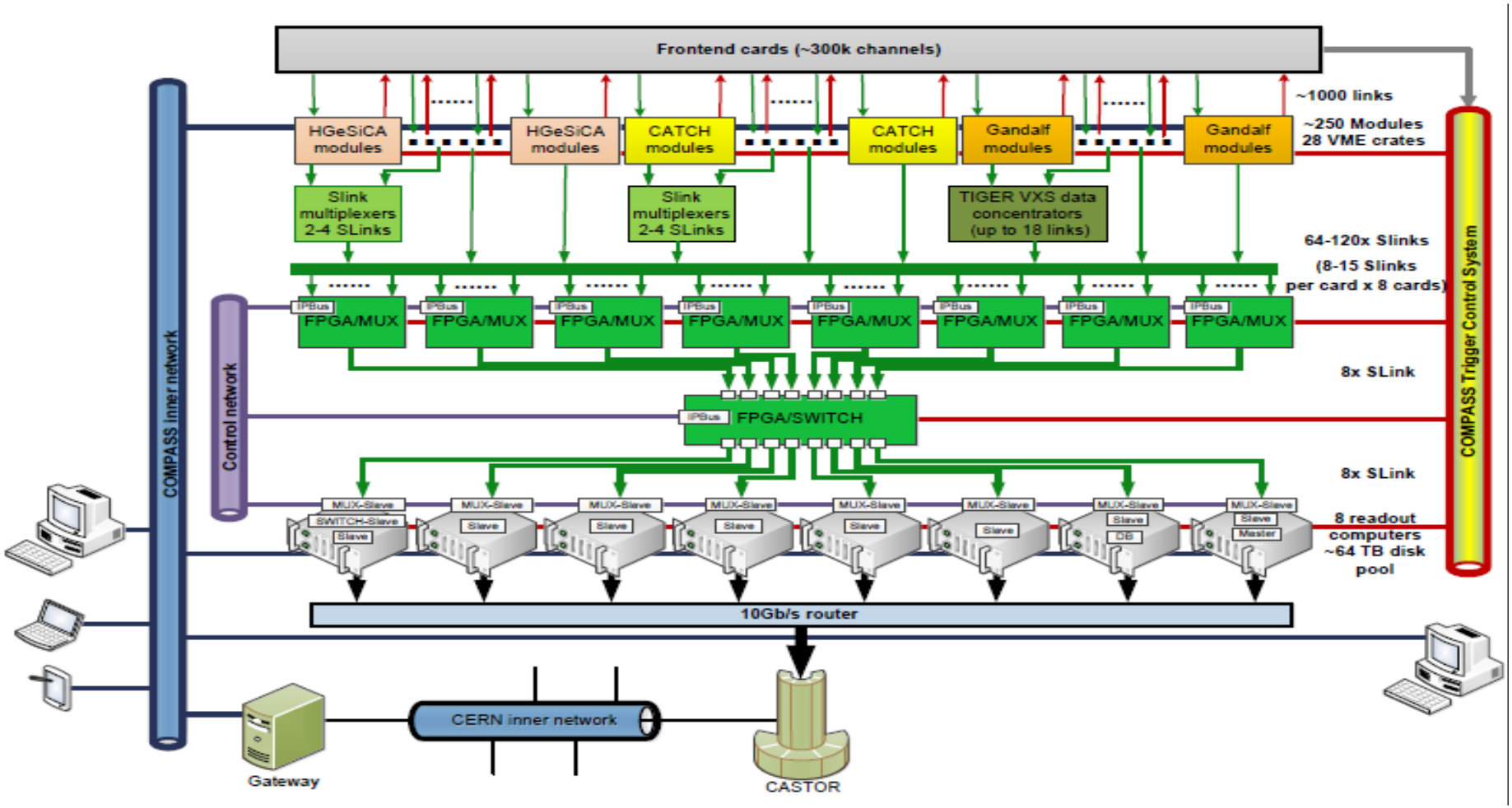
Networking: EVB traffic



Event Building dilemma

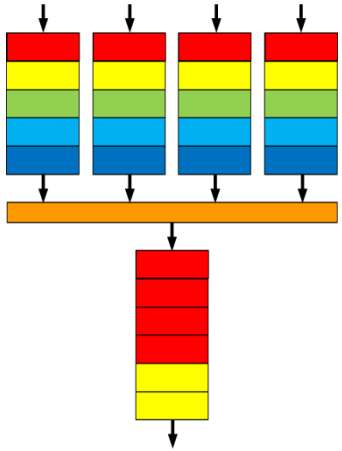
For Event builder traffic pattern congestion is a problem...

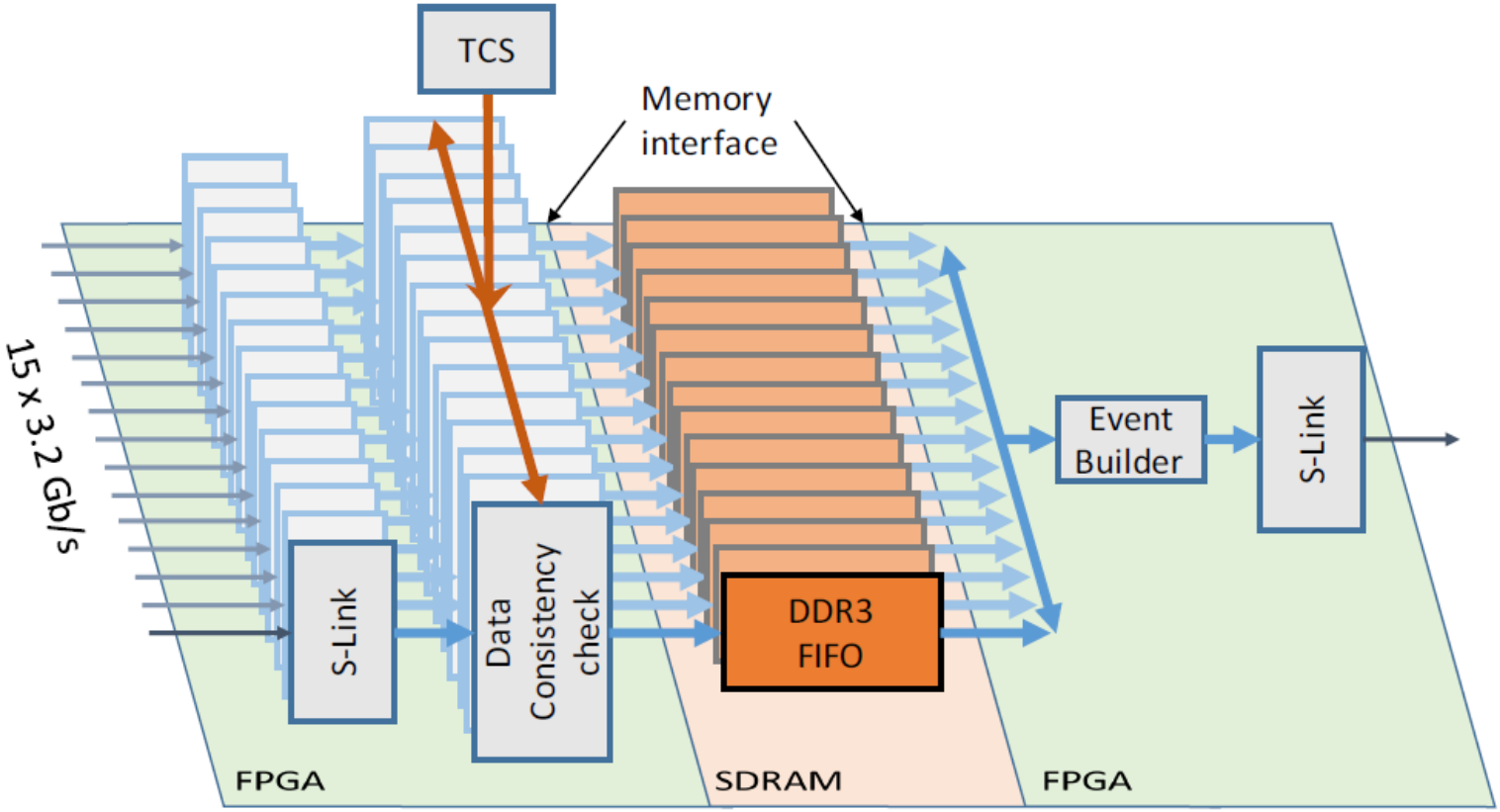
COMPASS iFDAQ



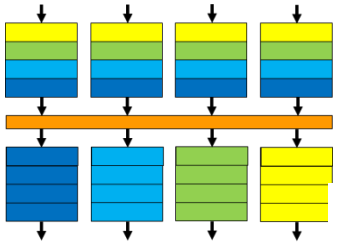
8 PC + 9 FPGA event building modules

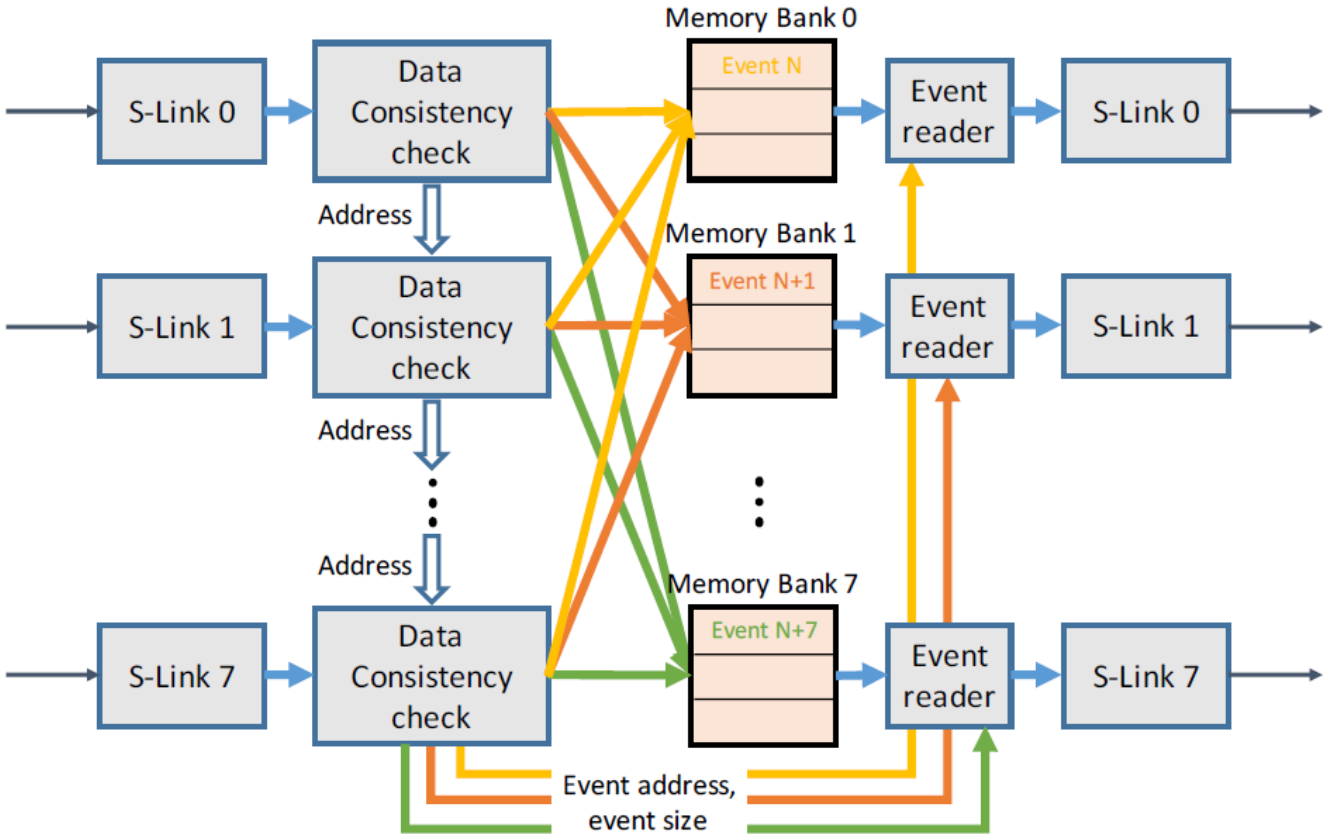
Event Multiplexer



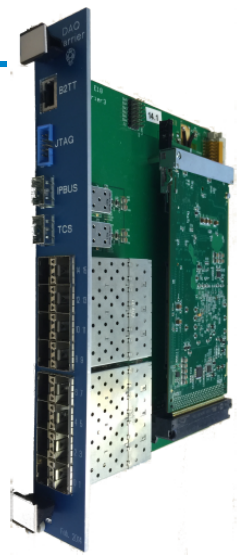


Event Switch





iFDAQ hardware



- Three interfaces:
  - Time distribution - TCS
  - Slow Control/Monitoring(IPBUS)
  - Data interface(Slink)

- On spill Data Rate : 1.5 GB/s
- Sustained rate : 500 MB/s
- Maximum sustained rate 2.5-3 GB/s
- Data buffering on all levels =>

Self synchronized data flow

- Intelligence – road to future
  - Data consistency check
  - Error diagnostics
  - Resynchronization of FE modules
  - Data Throttling
  - Reconfiguration to over come

Conclusions

- Modern FPGA support all type of interfaces needed to build FE electronics and DAQ wo external components
- Pool of standard interfaces minimizes firmware and software development time
- iFDAQ reliable and simple FPGA based event builder architecture

THANK YOU